



Maestría en Ingeniería en Automatización de Procesos Industriales

Title

**Implementation of hysteresis current control in an
FPGA and the power stage to regulate the speed of
a three phase synchronous brushless dc motor**

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Implementation of a hysteresis current control in an FPGA and the power stage to regulate the speed of a three phases synchronous brushless dc motor



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1. Introduction

Brushless DC motor (BLDC) and the permanent magnet synchronous motor (PMSM) are used extensively in several applications, for example domestic, aerospace and automotive industries because of their characteristics such as high relative weight-torque, high efficiency, noiseless and simplicity in their control.

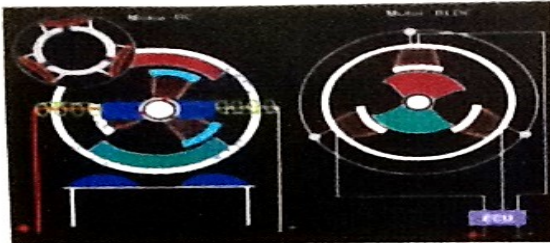


Figure 1. DC motor vs brushless DC motor

2. Objectives

2.1. General objective

Developing an experimental platform for speed control of three-phase synchronous brushless DC motor.

2.2. Specific objectives

- To simulate the complete system of a brushless dc motor that consisting of a power stage, controller and the hall effect sensors to determine its behavior at different speeds and torques in Matlab / Simulink.
- To design the power stage for switching a three-phase brushless DC motor up to 30 A.
- To implement the hysteresis current controller in VHDL language and integrate the system into an FPGA for the acquisition and generation of control signals.

3. Method

This section will discuss the steps and the diagrams used to implement the hysteresis current control and the direct torque Control .

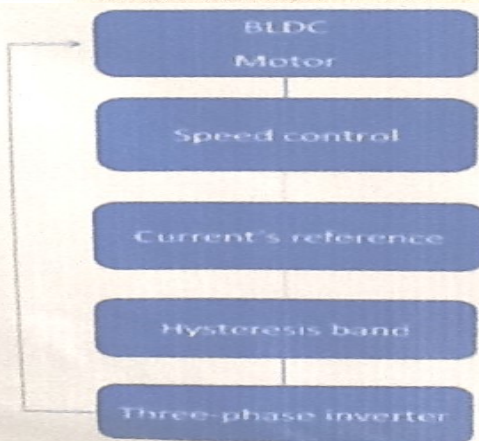


Figure 2. Methodology utilized in the current control.

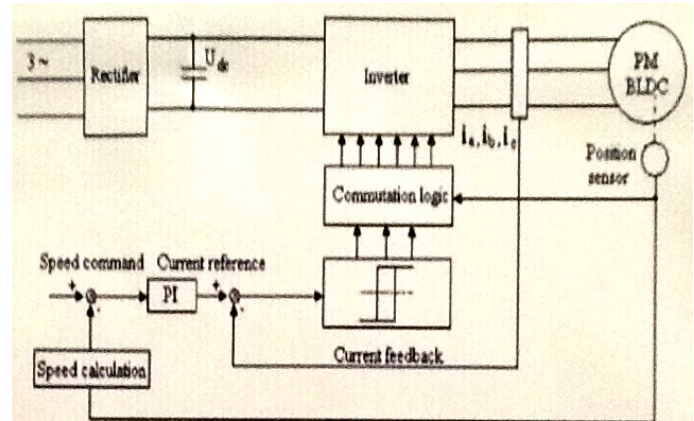


Figure 3. Schematic of conventional current control

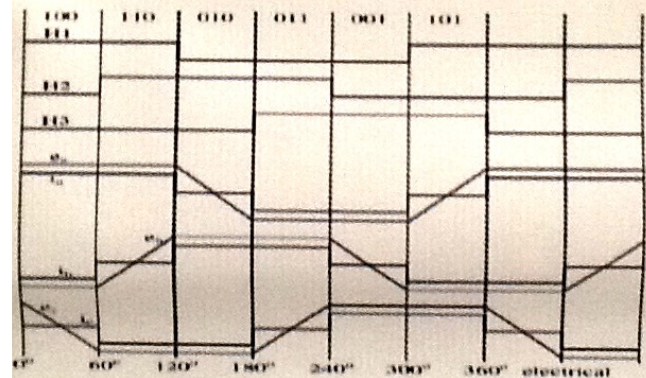


Figure 4. Ideal Back-Emf's, phase current and position sensor signals

Table 1. Selection switching for a BLDC motor

State	Hall effect sensors			PWM		Phase currents		
	A	B	C			A	B	C
1	0	0	1	Q1	Q4	DC+	Inactivo	DC-
2	0	0	0	Q1	Q2	DC+	DC-	Inactivo
3	1	0	0	Q5	Q2	Inactivo	DC-	DC+
4	1	1	0	Q5	Q0	DC-	Inactivo	DC+
5	1	1	1	Q3	Q0	DC-	DC+	Inactivo
6	0	1	1	Q3	Q4	Inactivo	DC+	DC-

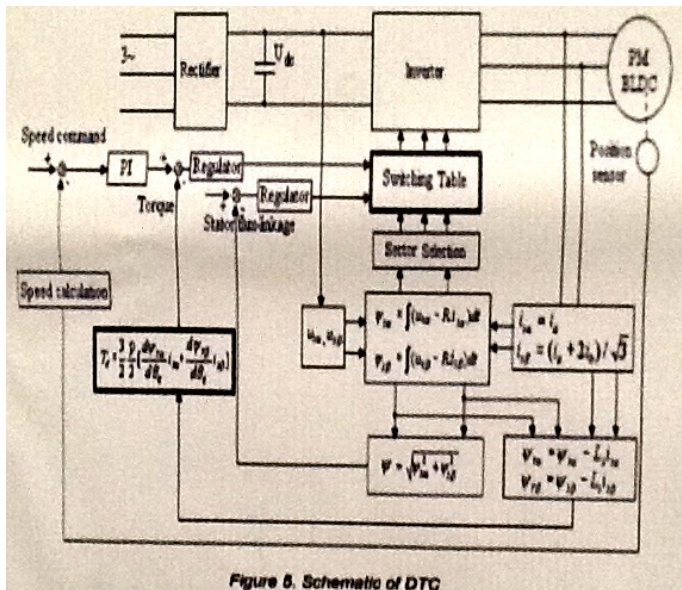


Figure 5. Schematic of DTC

Table 2. Voltage selection for a BLDC motor for DTC scheme

φ	τ	sector(s)					
		sector(1)	sector(2)	sector(3)	sector(4)	sector(5)	sector(6)
φ=1	τ=1	V ₂ =(110)	V ₃ =(010)	V ₄ =(011)	V ₅ =(001)	V ₆ =(101)	V ₁ =(100)
	τ=-1	V ₆ =(101)	V ₁ =(100)	V ₂ =(110)	V ₃ =(010)	V ₄ =(011)	V ₅ =(001)
φ=-1	τ=1	V ₃ =(010)	V ₄ =(011)	V ₅ =(001)	V ₆ =(101)	V ₁ =(100)	V ₂ =(110)
	τ=-1	V ₅ =(001)	V ₆ =(101)	V ₁ =(100)	V ₂ =(110)	V ₃ =(010)	V ₄ =(011)

4. Results

In the first two images we can see the two controllers implemented in Simulink meanwhile Figures 8 and 9 show the speed response of each controller and the figure 10 shows the experimental platform for a brushless DC motor.

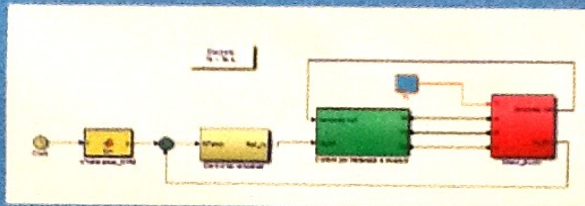


Figure 6. Simulink's schematic of current control

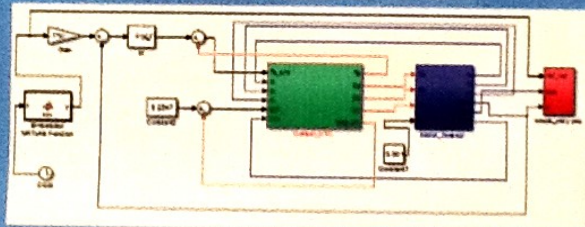


Figure 7. Simulink's schematic of DTC

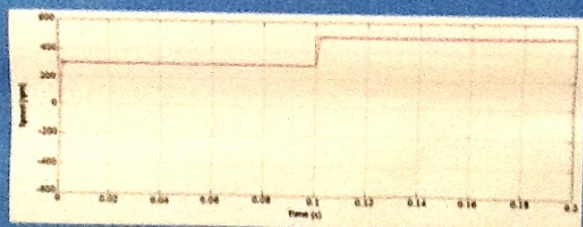


Figure 8. Velocity graph of current control

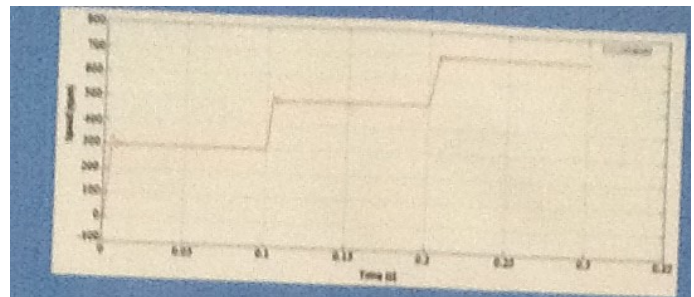


Figure 9. Velocity graph of DTC



Figure 10. Design of experimental platform into Solidworks

5. Conclusion

with the results shown in this presentation we concluded the first objective of the thesis therefore we can move into the co-simulation between active hdl / Simulink.

Acknowledgements

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