A state-variable filter with 2kHz-8kHz voltage-controlled center frequency based on ALD1106 quasi-floating-gate transistors

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Abstract

A state variable filter with center frequency tuning capability is presented. Tuning is achieved by means of voltage-controlled integrators based on quasi-floating-gate transistors. An experimental prototype realized with three operational amplifiers, six capacitors, four resistors and four ALD1106 NMOS transistors presented tuning capability from 2kHz to 8kHz, with 0.28% of Total Harmonic Distortion in the low-pass response when an input of amplitude 0.2V and frequency 0.1kHz was employed.

1. Introduction

Analog filters are employed in biomedical signal processing to reject unwanted flicker or out band noises. The bandwidth of those signals is typically in the range from 0.1Hz to 10kHz. Consequently, programmability is desirable [1]. Unfortunately, the design of programmable integrated filters with bandwidths below 1kHz is not a trivial task, especially if other design specifications, such as low noise, low distortion, small area and reduced power consumption must be satisfied. The challenge comes from the lack of large time constants. To overcome this lack some strategies have been used in the literature, among them [2-3]: Off-chip capacitors (additional output pads); Capacitance multiplication (coarse programmability with discrete control); Current division and current cancellation (prone to present mismatch and large offset components); Log-domain processing, (the input is compressed, nonlinearly processed, and expanded at the output) [4-6]. The main disadvantages of those approaches are the large area required and/or the lack of tuning capability. This way, in this work we propose a compact realization of a tunable filter suitable for biomedical applications. It is based on programmable active resistors biased using a modified version of the quasi-floating gate transistor (QFGT), which intends reduce area requirements. These active resistors can be tuned by means of a DC voltage, avoiding the need of large capacitors. The filter is verified by means of a discrete implementation with ALD1106 transistors.

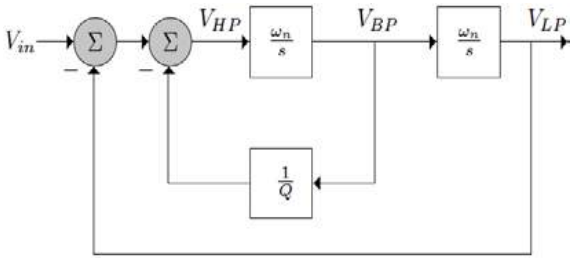

Fig. 1. State-variable filter (block diagram).

2. Proposed Tunable Filter

2.1. State-variable filter

The biquad state-variable RC active filter is based on the method of solving differential equations. The topology of this filter is such that, depending upon where the circuit is tapped as an output, low-pass, band-pass, or high-pass characteristics can be realized with low sensitivities [7]. Besides, the quality factor Q and the natural frequency ω_n can be set separately. This flexibility comes from the filter's implementation, which requires two adders, two integrators and two gain blocks, as is shown in Fig 1. In this diagram, the three outputs V_{HP}, V_{BP} and V_{LP} represent the high-pass, band-pass and low-pass responses, respectively. The corresponding transfer functions become

$$H_{HP}(s) = \frac{s^2}{s^2+\frac{\omega_n}{Q}s+\omega_n^2}$$
$$H_{BP}(s) = \frac{\omega_n s}{s^2+\frac{\omega_n}{Q}s+\omega_n^2} \quad (1)$$
$$H_{LP}(s) = \frac{\omega_n^2}{s^2+\frac{\omega_n}{Q}s+\omega_n^2}$$

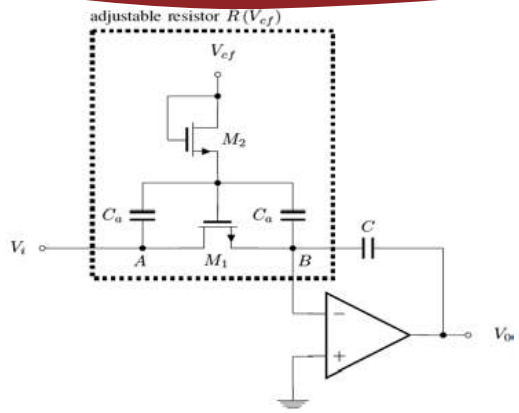

Fig. 2. Gain-adjustable inverter integrator.

2.2. Programmable inverter integrator

Integrator architectures use operational amplifiers with capacitive feedback to integrate the applied signal. In order to build a programmable filter, the transfer function of the integrators must be adjustable. This characteristic is achieved by employing the integrator depicted in Fig. 2 with an adjustable voltage-controlled active resistor $R(V_{cf})$ controlled by the DC voltage V_{cf}. The corresponding transfer function results

$$H(s) = -\frac{1}{sCR(V_{cf})} \tag{2}$$

2.3. Tunable resistor $R(V_{cf})$

The proposed implementation of $R(V_{cf})$ is similar to the reported in [8]. It consists of the channel resistance of transistor M_1, biased to operate in triode mode with

$$R(V_{cf}) = \frac{1}{\beta(V_{cf}-V_B-V_{Tn})} \tag{3}$$

where $\beta=\mu_n C_{OX}(W/L)$, V_{Tn} and V_B are the transconductance factor, threshold voltage and source voltage of the transistor M_1, respectively. To save area, a diode-connected NMOS transistor M_2 replaces the PMOS transistor of the conventional NMOS QFGT in order to reduce the number of required N-wells. This way, the quiescent control voltage V_{cf} is established in the gate of M_1 by the large drain to source resistance of M_2, r_{ds2}, which operates in weak inversion mode because of its source terminal is connected to the gate of M_1. Therefore, $r_{ds2}=1/g_{mM2}\approx U_T/I_{leakage}$ and $r_{ds2}>>R(V_{cf})$, where $U_T\approx$25mV @ 300ºK and $I_{leakage}$ is the leakage current in the gate of M_2. Regrettably, M_1 working in triode mode presents a significant distortion motivated by the drain-to-source voltage drop and the body effect. It can be linearized using the "common-mode" linearization technique [8], which is performed by M_2 and the two capacitors C_a. In this array, the average of the voltages in the drain and source of M_1 is added to the gate voltage of M_1 through the capacitors C_a. This way, the gate voltage of M_1 becomes $v_{GM1}=(v_A+v_B)/2+V_{cf}$. Also, the DC components of voltages at nodes A and B do not affect de DC components of v_{GM1} because of the presence of the two high-pass RC filters r_{ds2}-C_a. For a sinusoidal input with amplitude A, the second- and third- harmonic distortion factors of I_{DM1} become [9]

$$HD_2 = \frac{A}{2}\left|\frac{\gamma/(4\sqrt{V_B+2\phi_F})}{T-0.5V_A}\right|$$
$$HD_3 = \frac{A^2}{96}\left|\frac{\gamma}{(V_A+2\phi_F)^{3/2}[T-0.5V_A]}\right| \tag{4}$$

where $T=V_{cf}-V_{FB}-2\phi_F-\gamma(V_A-2\phi_F)^{0.5}$, V_{FB} is the flat-band voltage, the γ body-effect parameter, ϕ_F the Fermi level and V_A the drain voltage of M1. Typical values of HD_2 and HD_3 are in the range from 1% to 2%.

2.4. Circuit approximation

Fig. 3 shows the circuit approximation of the block diagram of Fig. 1. The first integrator is conformed by a resistor $R(V_{cf})$, a capacitor C and the operational amplifier OA_2. The second integrator is realized with a resistor $R(V_{cf})$, a capacitor C and the amplifier OA_3. The two adders of Fig. 1 are implemented with the differential amplifier conformed by the resistors R_2 and R_3, the two resistors R_1, and the amplifier OA_1. By performing nodal analysis, the high-pass (H_{HP}), band-pass (H_{BP}) and low-pass (H_{LP}) responses become

$$H_{HP}(s) = \frac{\frac{2R_2}{R_2+R_3}s^2}{s^2+\frac{R_3}{R_2+R_3}\frac{1}{RC}s+\frac{1}{R^2C^2}}$$
$$H_{BP}(s) = \frac{-\frac{2R_2}{R_2+R_3}\frac{1}{RC}s}{s^2+\frac{R_3}{R_2+R_3}\frac{1}{RC}s+\frac{1}{R^2C^2}} \tag{5}$$
$$H_{LP}(s) = \frac{\frac{2R_2}{R_2+R_3}\frac{1}{R^2C^2}}{s^2+\frac{R_3}{R_2+R_3}\frac{1}{RC}s+\frac{1}{R^2C^2}}$$

with maximum gains given by

$$\left|H_{HP(s=\infty)}\right| = \left|H_{LP(s=0)}\right| = \frac{2R_2}{R_2+R_3}$$
$$\left|H_{BP(s=j\omega_n)}\right| = \frac{R_2}{R_3} \tag{6}$$

and with natural frequency ω_n and quality factor Q

$$\omega_n = \frac{1}{R(V_{cf})C}$$
$$Q = \frac{1}{2}\left(1+\frac{R_2}{R_3}\right) \tag{7}$$

f_n is tuned by modifying $R=R(V_{cf})$ through V_{cf}.

2.5 Effect of the linearization

The linearization introduces parasitic influences that affect the transfer functions given by (5). To evaluate these effects it is assumed $C_a>>C_{par}$ and $r_{ds2}>>\max(R(V_{cf}), R_1, R_2, R_3)$, where C_{par} represents any

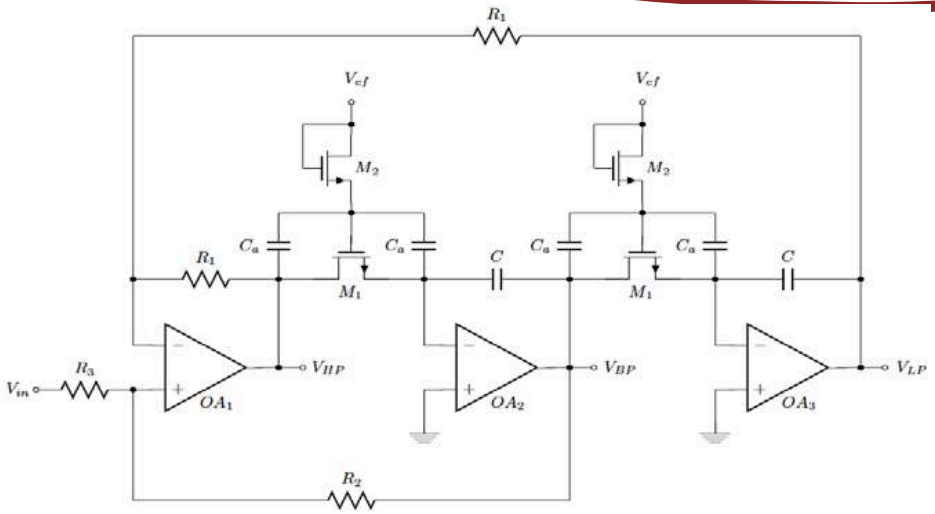

Fig. 3. Proposed state-variable filter with electrically tunable center frequency.

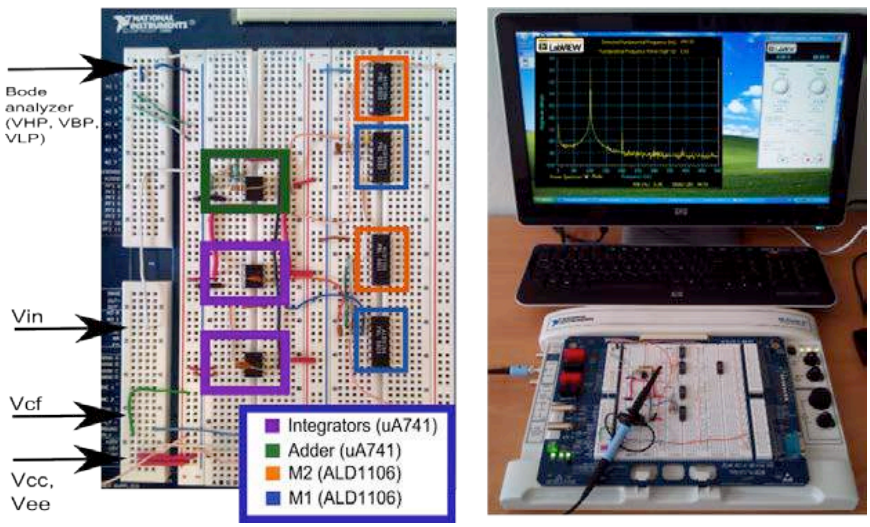

Fig. 4. Experimental setup.

Table 1. Design details.

Element	Value
R_1, R_2, R_3, C, C_a	1KΩ, 10KΩ, 1.2KΩ, 0.1μF, 1nF

of the parasitic capacitances associated with M_1 and M_2. If r_{ds2} is considered an open circuit, then each pair of capacitors C_a can be replaced by one capacitor of value $0.5C_a$ in parallel with $R(V_{cf})$. Using this model can be demonstrated that the linearization array introduces a two-multiplicity zero z. However, if $C>>C_a$ then the parasitic zeros are shifted far-off ω_n and the effect of the linearization technique over ω_n and Q results negligible because of

$$\left|\frac{z}{\omega_n}\right| = \frac{2C}{C_a}\sqrt{1+\frac{C_a}{2C}} \gg 1$$
$$\frac{\omega_n|_{ideal-R}}{\omega_n|_{linearized-R}} = \frac{1}{\sqrt{1+\frac{C_a}{2C}}} \approx 1 \qquad (8)$$
$$\frac{Q|_{ideal-R}}{Q|_{linearized-R}} = \frac{\sqrt{1+\frac{C_a}{2C}}}{\sqrt{1+\frac{C_a}{C}}} \approx 1$$

3. Experimental Validation

A prototype of the proposed filter was implemented with discrete components. Fig. 4 shows the circuit evaluation test-setup and Table 1 the design details. The operational amplifiers occupied were uA741 with open loop gain of 106dB and minimum Gain Bandwidth Product (GBW) of 1MHz. Resistors with tolerance of 10% and ceramic capacitors were also used. The transistors employed were ALD1106 NMOS transistors with threshold voltage of 0.7V. Four packages were utilized to avoid body effect. Since the maximum test frequency of the circuit was established as 100kHz the components were mounted on a protoboard. The test-setup consisted of the Educational Laboratory Virtual Instrumentation Suite of National Instruments (ELVIS-II), which handed ±12V for biasing the OPAMPs and established the control signal V_{cf}. The AC response and the harmonic distortion of the filter were characterized using the Bode Plotter and the Dynamic Analyzer of the ELVIS-II.

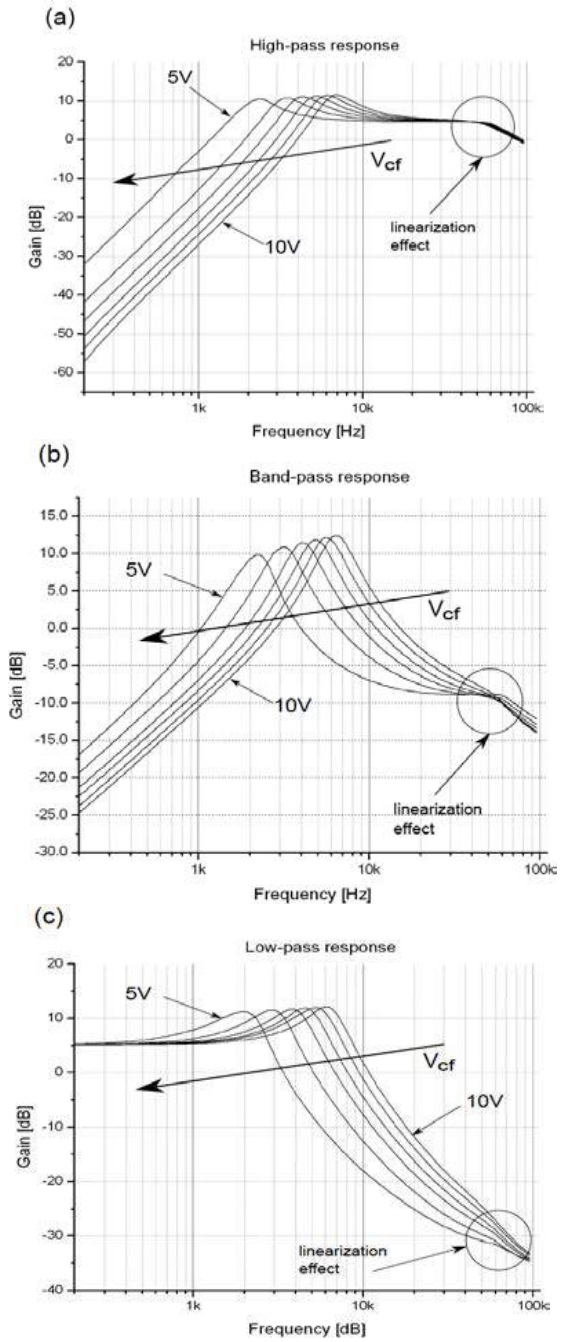

Fig. 5. Experimental results: (a) V_{HP} response; (b) V_{BP} response; (c) V_{LP} response.

The frequency responses of the $V_{HP}(s)$, $V_{BP}(s)$ and $V_{LP}(s)$ signals are illustrated in Fig. 5. The amplitude of the input signal was 0.2V. Sweeping V_{cf} from 5V to 10V in increments of 1V was obtained a range of the f_n from 2kHz to 8kHz with a maximum deviation of the linearity of 3.4% (see Fig. 6). It corresponds to a tuning range of $R(V_{cf})$ from 636KΩ to 227KΩ (see Fig. 7). With R_2=10KΩ and R_3=1.2KΩ were calculated $|H_{BP}(s=j\omega_{\square})|$=18dB and $|H_{HP}(s=\infty)|=|H_{LP}(s=0)|$=5dB, but the measured gains resulted 12.5dB and 5dB. This discrepancy is due to the Q reduction caused by the linearization scheme, which is worsened by the large parasitic capacitances of the protoboard.

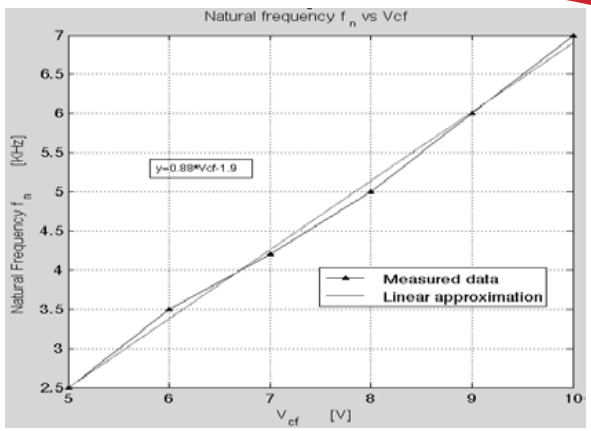

Fig. 6. Natural frequency f_n vs V_{cf}.

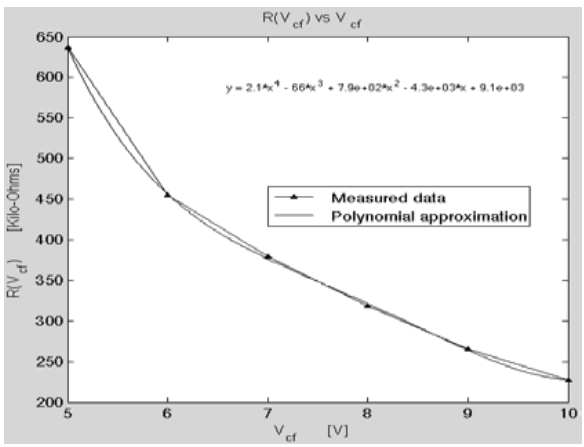

Fig. 7. Equivalent resistance $R(V_{cf})$ vs V_{cf}.

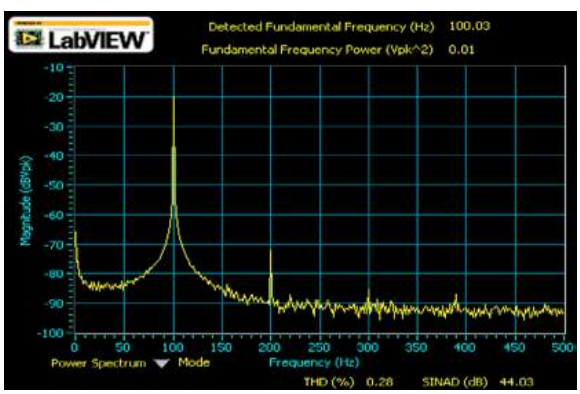

Fig. 8. Harmonic distortion of signal $V_{LP}(s)$.

The measured Total Harmonic Distortions (THD) of the low-pass output is shown in Fig. 8. It resulted 0.28% for an input of amplitude 0.2V and frequency 0.1kHz, with the f_n centered at 2kHz.

In Table II some integrated tunable filters proposed in the literature are compared with the discrete implementation of this work. As can be noticed, the tuning range of the proposed filter is less than one decade. However, this range was imposed by the use of discrete components, which allows operate $R(V_{cf})$ in strong inversion mode. A filter with multidecade tuning range can be obtained by incorporating weak

Table 2. Design details.

Reference and CMOS process	Technique	Tunable range
[2] (1.2µm)	Current division, capacitance multiplication	2Hz
[4] (1.2µm)	Log domain Large floating-gate transistors	1Hz-100kHz
[6] (0.8µm)	Log domain	25Hz-35kHz
[10] (0.18µm)	Current steering	12Hz-200Hz
[11] (0.18µm)	PMOS in subthreshold region	3Hz-106kHz
This work	quasi-floating-gate transistors	2kHz-8kHz

inversion operation by means of an integrated circuit realization [11]. Also, regarding the other filters of Table II, the proposed circuit does not require capacitance multipliers or current cancellation techniques, reducing design effort, power consumption and area requirements.

4 Conclusions

A state-variable tunable filter has been introduced and verified experimentally. The filter incorporates voltage-controlled tunable active resistors, allowing a compact realization with low hardware complexity. This discrete implementation can be improved with an integrated circuit version to obtain multidecade tuning without employing other techniques for low frequency filtering, such as the use of capacitance multipliers or current division/cancellation techniques.

5. Acknowledgment

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