Maestría en Ingeniería en Automatización de Procesos Industriales

Title

Cascade fractional-order phase-lag control of DC-DC boost converters applied in photovoltaic solar systems

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Cascade Fractional-Order Phase-Lag Control of DC-DC Boost Converters applied in Photovoltaic Solar Systems

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1. Introduction

Switched power converters is a challenging area of research in control engineering. DC-DC boost converters have become essential components in many power source applications, such as photovoltaic solar systems, requiring complex control circuitry in order to account for load variations, component tolerances, external perturbations, system aging and input source voltage [1]. Several strategies have been reported to satisfy these requirements, been the most important integer and fractional order PIDs [1] and sliding-mode controllers [2]. Fractional-order controllers present better transitory response that their integer-order or sliding-mode counterparts [1], but it is required numerical optimization of simultaneous non-linear inequality. This work avoids this disadvantage by means of fractional-order lag compensators, which have unique and exact solution by means on only algebraic manipulation.

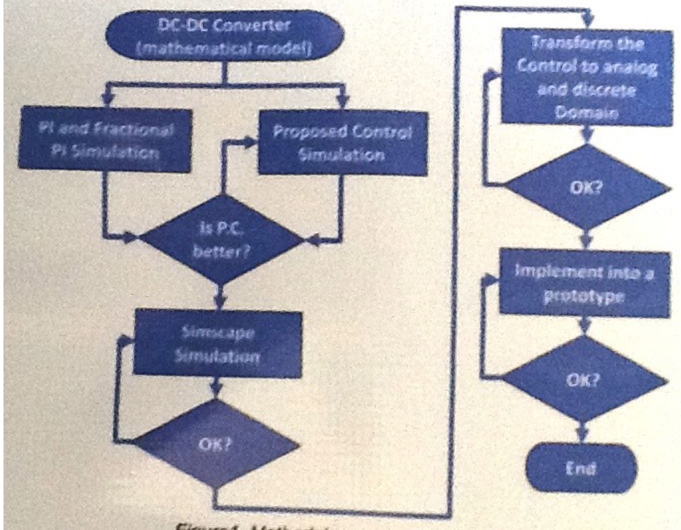
2. Objectives

2.1. General objective

To establish a methodology for the implementation in reconfigurable hardware of cascade-mode fractional-order lead-lag compensators to reduce the overshoot and perturbation effects over the response of DC-DC Boost converters in photovoltaic solar systems and compare it with other reported control strategies.

2.2. Particular objectives

- To obtain the mathematical model of the Boost converter in the photovoltaic solar system and compare by means of MATLAB simulation its control with diverse strategies, including the proposed fractional-order compensators.
- To establish a methodology for the analog and digital implementation in reconfigurable hardware of the proposed controllers.
- To validate experimentally the proposed methodologies by means of a physical prototype.



DC-DC Converter (mathematical model)

PI and Fractional PI Simulation

Proposed Control Simulation

Is P.C. better?

Simscape Simulation

OK?

Transform the Control to analog and discrete Domain

OK?

Implement into a prototype

OK?

End

Figure1. Methodology employed

4. System description

The parameters of the Boost converter of Figure 2 are shown in Table 1 [1]. It requires a specific input voltage (60V) known as "Reference Voltage" which increases to a desired "Output Voltage" equal to 120V.

Table 1. Boost Converter specifications.

Parameter	Value
Input Voltage (Vin)	60 V
Output Voltage (Vo)	120 V
OutputPower	120 W
Load Resistor (R)	120 Ω
Capacitance (C)	400 µf
Inductance (L)	2.5 mH
Switching Frequency (fs)	40 KHz
Duty Cycle	0.5

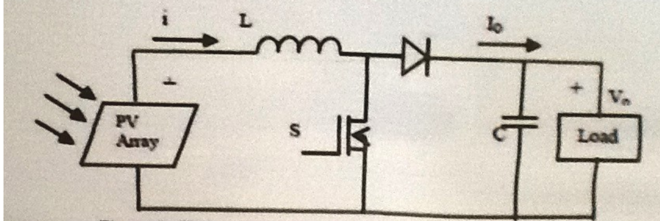


Figure 2. Electrical diagram of Boost converter built in Simulink.

In the cascade-mode control structure of Figure 3 *Gid* and *Gvoil* are the plants, *Gci* is the inner loop control and *Gcv* is the outer loop control.

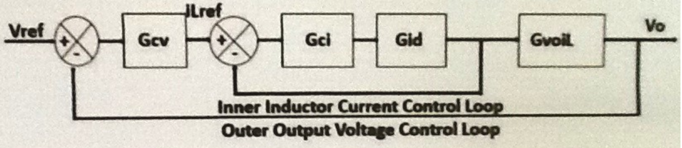


Figure 3. Electrical diagram of Boost converter built in Simulink.

$$\frac{i_L(s)}{d(s)} = Gid = \frac{4.8x10^4 s+1.818x10^6}{s^2+18.94s+2.273x10^5} \qquad GvoiL(s) = \frac{R}{RCs+1} = \frac{120}{0.048s+1}$$

$$C_f(s) = K\left(\frac{1+\alpha\tau s^q}{1+\tau s^q}\right)$$

$$\alpha = \frac{uv\tan\left(\frac{q\pi}{2}\right)-1}{v\tan\left(\frac{q\pi}{2}\right)-1} \qquad \tau = \frac{1}{\omega_c^q}\left[v\sin\left(\frac{q\pi}{2}\right) - \cos\left(\frac{q\pi}{2}\right)\right]$$

$$u = c\frac{c-\cos(p)}{c\cos(p)-1} \qquad v = \frac{c\cos(p)-1}{c\sin(p)}$$

$$q = \left\{\begin{array}{cc} 2+\frac{2}{\pi}\tan^{-1}\left(\frac{u_0-K}{v(u_0-Ku)}\right) & si \quad v(u_0-Ku)>0 \\ 1 & si \quad v(u_0-Ku)=0 \\ \frac{2}{\pi}\tan^{-1}\left(\frac{u_0-K}{v(u_0-Ku)}\right) & si \quad v(u_0-Ku)<0 \end{array}\right\}$$

PI controller [ ]:

$$G_{ci}(s) = \frac{2172(1+0.00014s)}{s}, \qquad G_{cv}(s) = \frac{61.15(1+0.0041s)}{s}$$

Fractional-order PI controller [ ]:

$$G_{cv}(s) = 0.30408 + 2172\left(\frac{0.333s+1}{s+0.333}\right), \quad G_{ci}(s) = 0.25 + 61.15\left(\frac{0.333s+1}{s+0.333}\right)$$

Proposed integer-order phase-lag compensator:

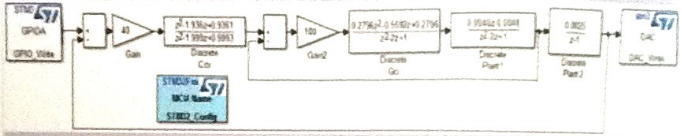
$$G_{ci}(s) = \frac{0.0075s + 100}{0.014s + 1}, \qquad G_{cv}(s) = \frac{0.0854s + 40}{0.2311s + 1}$$

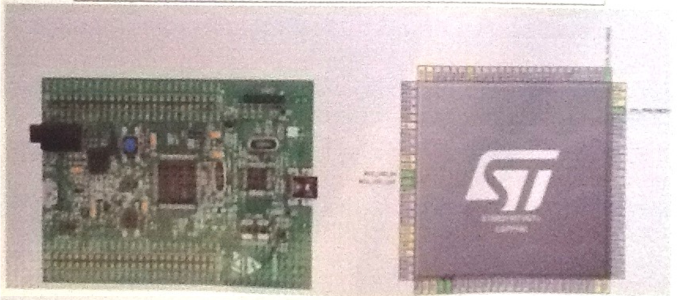
Proposed fractional-order phase-lag compensator:

$$G_{ci}f(s) = 100\left(\frac{0.274s^2 + 6.79s + 4.93}{0.98s^2 + 7.76s + 4.97}\right), \quad G_{cv}f(s) = 40\left(\frac{s^2 + 639.75s + 948.96}{s^2 + 7.06s + 9.489}\right)$$

Methodology for digital implementation

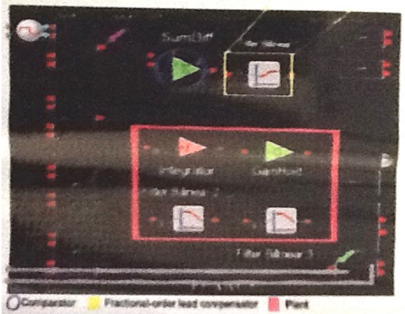
Generate a new project in STM32CubeMX, declaring the ports to use [3]. Build in Simulink the system model to control. Simulate to verify the right operation. Generate C code from Simulink by clicking "Build Model" button, then Keil will be open automatically. For default Keil µVision 5 recognizes the model of the board in use. From "Options for Target" select the "ST-Link Debugger". In "Programming Algorithm" option select "STM32F4xx Flash". Compile the program. If there are no errors download it on the card with the "Download" button. Finally, take lecture from the outputs of the DAC to compare it with the simulation results.





Methodology for analog implementation

Fractional-order phase lag controllers are approximated with bi-quad filters and implemented using Field Programmable Analog Arrays (FPAA) [4].



$$C(s) = \frac{1+\alpha\tau s^q}{1+\tau s^q} = \alpha\left(\frac{s^2 + \frac{\omega_z}{Q_z}s + \omega_z^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}\right)$$

5. Results

A Cascade-Mode control for a Boost converter built in Simulink that only needs to replace Outer and Inner loops control with different control methodologies is shown in Fig. 5.

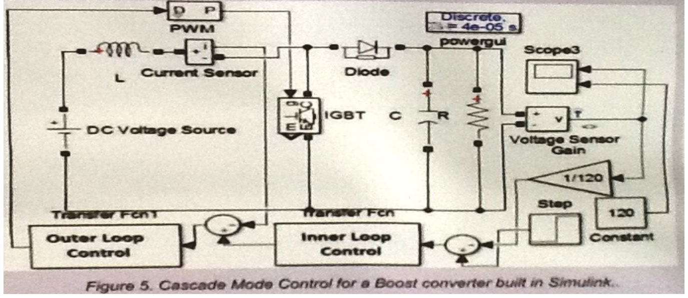


Figure 5. Cascade Mode Control for a Boost converter built in Simulink.

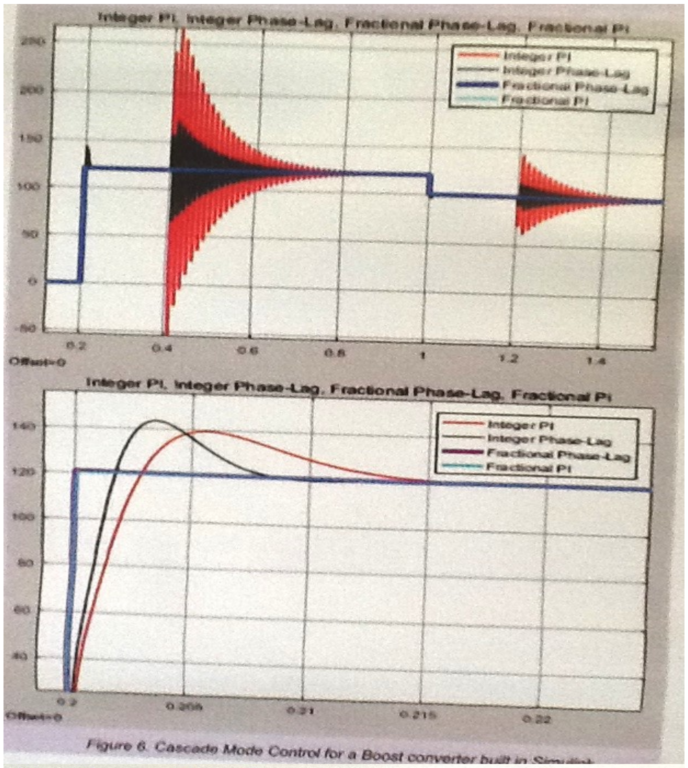


Figure 6. Cascade Mode Control for a Boost converter built in Simulink.

6. Conclusion

According to obtained results we can conclude that fractional order design techniques have better performance than their counterparts in integer order. In the previous plots is shown how the fractional responses are faster than integer order and the overshoot was reduced 23% with fractional compensators. The fractional order in both, inner currnet-mode and external voltage-mode loops improves the transitory response and the disturbance rejection. Contrary to fractional-order PID controllers, the parameters of the compensator can be algebraically obtained in an exact and unique fashion, without numerical optimization.

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